## IN THE TITLE

Please amend the title as follows:

~~DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY~~ MEMORY DEVICE

## IN THE SPECIFICATION

**At page 3, line 27, please add the following:**

REFERENCES

B. Dipert et al., "Flash Memory Goes Mainstream," IEEE Spectrum, pp. 48-52 (Oct. 1993);

S.M. Sze, "Physics of Semiconductor Devices," John Wiley & Sons, New York (1969), p. 496;

S.R. Pollack et al., "Electron Transport Through Insulating Thin Films," Applied Solid State Science, Vol. 1, Academic Press, New York, (1969), p. 354;

D.A. Baglee, "Characteristics and Reliability of 100 Å Oxides," Proc. 22nd Reliability Symposium, (1984), p. 152;

G. Comapagnini et al. "Spectroscopic Characterization of Annealed $Si_{1-x}C_x$ Films Synthesized by Ion Implantation," J. of Materials Research, Vol. 11, No. 9, pp. 2269-73, (1996);

A. L. Yee et al. "The Effect of Nitrogen on Pulsed Laser Deposition of Amorphous Silicon Carbide Films: Properties and Structure," J. Of Materials Research, Vol. 11, No. 8, pp. 1979-86 (1996);

C. D. Tucker et al. "Ion-beam Assisted Deposition of Nonhydrogenated a-Si:C films," Canadian J. Of Physics, Vol. 74, No. 3-4, pp. 97-101 (1996);

H. Zhang et al., "Ion-beam Assisted Deposition of Si-Carbide Films," Thin Solid Films, Vol. 260, No. 1, pp. 32 -37 (1995);

S. P. Baker et al. "D-C Magnetron Sputtered Silicon Carbide," Thin Films, Stresses and Mechanical Properties V. Symposium, pp. Xix+901, 227-32 (1995);

N. N. Svirkova et al. "Deposition Conditions and Density-of-States Spectrum of a-$Si_{1-x}C_x$:H Films Obtained by Sputtering," Semiconductors, Vol. 28, No. 12, pp. 1164-9 (1994);

Y. Suzaki et al. "Quantum Size Effects of a-Si(:H)/a-SiC(:H) Multilayer Films Prepared by RF Sputtering," J. Of Japan Soc. Of Precision Engineering, Vol. 60, No. 3, pp. 110-18 (1996);

I. Pereyra et al. "Wide Gap a-$Si_{1-x}C_x$:H Thin Films Obtained Under Starving Plasma Deposition Conditions," J. Of Non-crystalline Solids, Vol. 201, No. 1-2, pp. 110-118 (1995);

A. S. Kumbhar et al. "Growth of Clean Amorphous Silicon Carbon Alloy Films By Hot-Filament

Assisted Chemical Vapor Deposition Technique," Appl. Phys. Letters, Vol. 66, No. 14, pp. 1741-3 (1995);

J. H. Thomas et al. "Plasma Etching and Surface Analysis of a-SiC:H Films Deposited by Low Temperature Plasma Enhanced Vapor Deposition," Gas-phase and Surface Chemistry in Electronic Materials Processing Symposium, Materials Research Soc., pp. Xv+556, 445-50 (1994);

Y. Yamaguchi et al. "Properties of Heteroepitaxial 3C-SiC Films Grown by LPCVD", 8th International Conference on Solid-State Sensors and Actuators and Eurosensors IX, Digest of Technical Papers, page 3. vol. (934+1030+85), pages 190-3, Vol. 2, 1995;

M. Andrieux, et al. "Interface and Adhesion of PECVD SiC Based Films on Metals", Le Vide Science, Technique et Applications. (France), No. 279, pages 212-214, 1996;

F. Lanois, "Angle Etch Control for Silicon Power Devices", Applied Physics Letters, Vol 69, No. 2, pages 236-238, July 1996;

N. J. Dartnell, et al. "Reactive Ion Etching of Silicon Carbide," Vacuum, Vol. 46, No. 4, pages 349-355, 1955;

R. Martins et al."Transport Properties of Doped Silicon Oxycarbide Microcrystalline Films Produced By Spatial Separation Techniques," Solar Energy Materials and Solar Cells, Vol. 41-42, pp. 493-517, June 1996;

R. Martins et al. "Wide band-gap microcrystalline silicon thin films," Diffusion and Defect Data Part B (Solid State Phenomena), Vol. 44-46, Pt. 2, pp. 299-346, 1995;

V. M. Bermudez et al. "The Growth and Properties of Al and AlN films on GaN" J. Appl. Physics, Vol. 79, No. 1, pp. 110-119 (1996);

I. Akasaki et al. "Effects of AlN Buffer Layer on Crystallographic Structure and On Electrical and Optical Properties of GaN and $Ga_{1-x}Al_xN$ Films Grown on Sapphire Substrate by MOVPE," J. Of Crystal Growth, Vol. 98, pp. 209-19, North Holland, Amsterdam (1989).

**The paragraph beginning at page 8, line 19 is amended as follows:**

The present invention discloses a memory cell such as, for example, a dynamic electrically alterable programmable read only memory (DEAPROM) cell. The memory cell has a

floating electrode, which is defined as an electrode that is "electrically isolated" from conductors and semiconductors by an insulator such that charge storage upon and removal from the floating electrode depends upon charge conduction through the insulator. In one embodiment, described below, the floating electrode is a floating gate electrode in a floating gate field-effect transistor, such as used in flash electrically erasable and programmable read only memories (EEPROMs). However, a capacitor or any other structure having a floating electrode and adjacent insulator could also be used according to the techniques of the present invention described below. According to one aspect of the present invention, a barrier energy between the floating electrode and the insulator is lower than the barrier energy between polycrystalline silicon (polysilicon) and silicon dioxide ($SiO_2$), which is approximately 3.3 eV. According to another aspect of the present invention, the shorter retention time of data charges on the floating electrode, resulting from the smaller barrier energy, is accommodated by refreshing the data charges on the floating electrode. In this respect, the memory operates similar to a memory cell in a dynamic random access memory (DRAM). These and other aspects of the present invention are described in more detail below.

**The paragraph beginning at page 9, line 8 is amended as follows:**

Figure **1** is a simplified schematic/block diagram illustrating generally one embodiment of a memory **100** according to one aspect of the present invention, in which reduced barrier energy floating electrode memory cells are incorporated. Memory **100** is referred to as a dynamic electrically alterable programmable read only memory (DEAPROM) in this application, but it is understood that memory **100** possesses certain characteristics that are similar to DRAMs and flash EEPROMs, as explained below. ~~For a general description of how a flash EEPROM operates, see B. Dipert et al., "Flash Memory Goes Mainstream," IEEE Spectrum, pp. 48-52 (Oct. 1993), which is incorporated herein by reference.~~ Memory **100** includes a memory array **105** of multiple memory cells **110**. Row decoder **115** and column decoder **120** decode addresses provided on address lines **125** to access the addressed memory cells in memory array **105**. Command and control circuitry **130** controls the operation of memory **100** in response to control signals received on control lines **135** from a processor **140** or other memory controller during

read, write, refresh, and erase operations. Command and control circuitry **130** includes a refresh circuit for periodically refreshing the data stored on floating gate transistor or other floating electrode memory cells **110**. Voltage control **150** provides appropriate voltages to the memory cells during read, write, refresh, and erase operations. Memory **100**, as illustrated in Figure **1**, has been simplified for the purpose of illustrating the present invention and is not intended to be a complete description. Only the substantial differences between DEAPROM memory **100** and conventional DRAM and flash EEPROM memories are discussed below.

**The paragraph beginning at page 12, line 26 is amended as follows:**

The Fowler-Nordheim tunneling current density in gate insulator **225**~~, which~~ is illustrated approximately by Equation **3** below~~, is described in a textbook by S.M. Sze, "Physics of Semiconductor Devices," John Wiley & Sons, New York (1969), p. 496~~.

$$J=AE^2e^{\left(-\frac{B}{E}\right)} \qquad (3)$$

In Equation **3**, J is the current density in units of amperes/cm$^2$, E is the electric field in gate insulator **225** in units of volts/cm and A and B are constants, which are particular to the material of gate insulator **225**, that depend on the effective electron mass in the gate insulator **225** material and on the barrier energy $\Phi_{GI}$. The constants A and B scale with the barrier energy $\Phi_{GI}$, as illustrated approximately by Equations **4** and **5**~~, which are disclosed in S.R. Pollack et al., "Electron Transport Through Insulating Thin Films," Applied Solid State Science, Vol. 1, Academic Press, New York, (1969), p. 354~~.

$$A\alpha\left(\frac{1}{\Phi_{GI}}\right) \qquad (4)$$

$$B\alpha(\Phi_{GI})^{\frac{3}{2}} \qquad (5)$$

For a conventional floating gate FET having a 3.3 eV barrier energy at the interface between the polysilicon floating gate and the $SiO_2$ gate insulator, A = 5.5 x $10^{-16}$ amperes/Volt$^2$ and B = 7.07

x $10^7$ Volts/cm~~, as disclosed in D.A. Baglee, "Characteristics and Reliability of 100 Å Oxides," Proc. 22nd Reliability Symposium, (1984), p. 152~~. One aspect of the present invention includes selecting a smaller barrier energy $\Phi_{GI}$ such as, by way of example, but not by way of limitation, $\Phi_{GI} \approx 1.08$ eV. The constants A and B for $\Phi_{GI} \approx 1.08$ eV can be extrapolated from the constants A and B for the 3.3 eV polysilicon-$SiO_2$ barrier energy using Equations **4** and **5**. The barrier energy $\Phi_{GI} \approx 1.08$ eV yields the resulting constants $A = 1.76 \times 10^{-15}$ amperes/Volt$^2$ and $B = 1.24 \times 10^7$ Volts/cm.

**The paragraph beginning at page 21, line 1 is amended as follows:**

An a-SiC inclusive gate insulator **225** can also be formed using other techniques. For example, in one embodiment gate insulator **225** includes a hydrogenated a-SiC material synthesized by ion-implantation of $C_2H_2$ into a silicon substrate **230**. ~~For example, see G. Comapagnini et al. "Spectroscopic Characterization of Annealed $Si_{1-x}C_x$ Films Synthesized by Ion Implantation," J. of Materials Research, Vol. 11, No. 9, pp. 2269-73, (1996).~~ In another embodiment, gate insulator **225** includes an a-SiC film that is deposited by laser ablation at room temperature using a pulsed laser in an ultrahigh vacuum or nitrogen environment. ~~For example, see A. L. Yee et al. "The Effect of Nitrogen on Pulsed Laser Deposition of Amorphous Silicon Carbide Films: Properties and Structure," J. Of Materials Research, Vol. 11, No. 8, pp. 1979-86 (1996).~~ In another embodiment, gate insulator **225** includes an a-SiC film that is formed by low-energy ion-beam assisted deposition to minimize structural defects and provide better electrical characteristics in the semiconductor substrate **230**. ~~For example, see C. D. Tucker et al. "Ion-beam Assisted Deposition of Nonhydrogenated a-Si:C films," Canadian J. Of Physics, Vol. 74, No. 3-4, pp. 97-101 (1996).~~ The ion beam can be generated by electron cyclotron resonance from an ultra high purity argon (Ar) plasma.

**The paragraph beginning at page 21, line 17 is amended as follows:**

In another embodiment, gate insulator **225** includes an a-SiC film that is synthesized at low temperature by ion beam sputtering in a reactive gas environment with concurrent ion irradiation. ~~For example, see H. Zhang et al., "Ion-beam Assisted Deposition of Si-Carbide~~

~~Films," Thin Solid Films, Vol. 260, No. 1, pp. 32–37 (1995).~~ According to one technique, more than one ion beam, such as an Ar ion beam, are used. A first Ar ion beam is directed at a Si target material to provide a Si flux for forming SiC gate insulator **225**. A second Ar ion beam is directed at a graphite target to provide a C flux for forming SiC gate insulator **225**. The resulting a-SiC gate insulator **225** is formed by sputtering on substrate **230**. In another embodiment, gate insulator **225** includes an SiC film that is deposited on substrate **230** by DC magnetron sputtering at room temperature using a conductive, dense ceramic target. ~~For example, see S. P. Baker et al. "D-C Magnetron Sputtered Silicon Carbide," Thin Films, Stresses and Mechanical Properties V. Symposium, pp. Xix+901, 227-32 (1995).~~ In another embodiment, gate insulator **225** includes a thin a-$Si_{1-x}C_x$:H film that is formed by HF plasma ion sputtering of a fused SiC target in an Ar-H atmosphere. ~~For example, see N. N. Svirkova et al. "Deposition Conditions and Density-of-States Spectrum of a-$Si_{1-x}C_x$:H Films Obtained by Sputtering," Semiconductors, Vol. 28, No. 12, pp. 1164-9 (1994).~~ In another embodiment, radio frequency (RF) sputtering is used to produce a-SiC films. ~~For example, see Y. Suzaki et al. "Quantum Size Effects of a-Si(:H)/a-SiC(:H) Multilayer Films Prepared by RF Sputtering," J. Of Japan Soc. Of Precision Engineering, Vol. 60, No. 3, pp. 110-18 (1996).~~ Bandgaps of a-Si, a-SiC, a-Si:H, and a-SiC:H have been found to be 1.22 eV, 1.52 eV, 1.87 eV, and 2.2 eV respectively.

**The paragraph beginning at page 22, line 10 is amended as follows:**

In another embodiment, gate insulator **225** is formed by chemical vapor deposition (CVD) and includes an a-SiC material. According to one technique, gate insulator **225** includes a-$Si_{1-x}C_x$:H deposited by plasma enhanced chemical vapor deposition (PECVD). ~~For example, see I. Pereyra et al. "Wide Gap a-$Si_{1-x}C_x$:H Thin Films Obtained Under Starving Plasma Deposition Conditions," J. Of Non-crystalline Solids, Vol. 201, No. 1-2, pp. 110-118 (1995).~~ According to another technique, mixed gases of silane and methane can be used to form a-$Si_{1-x}C_x$:H gate insulator **225**. For example, the source gas can include silane in methane with additional dilution in hydrogen. In another embodiment, gate insulator **225** includes a clean a-$Si_{1-x}C_x$ material formed by hot-filament assisted CVD. ~~For example, see A. S. Kumbhar et al. "Growth of Clean Amorphous Silicon Carbon Alloy Films By Hot-Filament Assisted Chemical~~

~~Vapor Deposition Technique," Appl. Phys. Letters, Vol. 66, No. 14, pp. 1741-3 (1995).~~ In another embodiment, gate insulator **225** includes a-SiC formed on a crystalline Si substrate **230** by inductively coupled plasma CVD, such as at 450 degrees Celsius, which can yield a-SiC rather than epitaxially grown polycrystalline or microcrystalline SiC. The resulting a-SiC inclusive gate insulator **225** can provide an electron affinity $\chi_{225} \approx 3.24$ eV, which is significantly larger than the 0.9 eV electron affinity obtainable from a conventional $SiO_2$ gate insulator. ~~For example, see J. H. Thomas et al. "Plasma Etching and Surface Analysis of a-SiC:H Films Deposited by Low Temperature Plasma Enhanced Vapor Deposition," Gas-phase and Surface Chemistry in Electronic Materials Processing Symposium, Materials Research Soc., pp. Xv+556, 445-50 (1994).~~

**The paragraph beginning at page 24, line 7 is amended as follows:**

In one embodiment, floating gate **215** is formed by CVD of polycrystalline or microcrystalline SiC, which can be either *in situ* conductively doped during deposition, or conductively doped during a subsequent ion-implantation step. According to one aspect of the invention, for example, floating gate **215** is formed of an SiC film that is deposited using low-pressure chemical vapor deposition (LPCVD). The LPCVD process uses either a hot-wall reactor or a cold-wall reactor with a reactive gas, such as a mixture of $Si(CH_3)_4$ and Ar. ~~Examples of such processes are disclosed in an article by Y. Yamaguchi et al., entitled "Properties of Heteroepitaxial 3C-SiC Films Grown by LPCVD", in the 8th International Conference on Solid-State Sensors and Actuators and Eurosensors IX, Digest of Technical Papers, page 3. vol. (934+1030+85), pages 190-3, Vol. 2, 1995, and in an article by M. Andrieux, et al., entitled "Interface and Adhesion of PECVD SiC Based Films on Metals", in supplement Le Vide Science, Technique et Applications. (France), No. 279, pages 212-214, 1996.~~ In other embodiments, floating gate **215** is formed of an SiC film that is deposited using other techniques such as, for example, enhanced CVD techniques known to those skilled in the art including low pressure rapid thermal chemical vapor deposition (LP-RTCVD), or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy (MBE). Other examples of forming SiC film floating gate **215** include reactive

magnetron sputtering, DC plasma discharge, ion-beam assisted deposition, ion-beam synthesis of amorphous SiC films, laser crystallization of amorphous SiC, laser reactive ablation deposition, and epitaxial growth by vacuum anneal. The conductivity of the SiC film of floating gate **215** can be changed by ion implantation during subsequent process steps, such as during the self-aligned formation of source/drain regions for the n-channel and p-channel FETs.

**The paragraph beginning at page 25, line 3 is amended as follows:**

In one embodiment, patterning and etching the SiC film, together with the underlying gate insulator **225**, forms the resulting individual SiC floating gates **215**. The SiC film is patterned using standard techniques and is etched using plasma etching, reactive ion etching (RIE) or a combination of these or other suitable methods. For example, the SiC film can be etched by RIE in a distributed cyclotron resonance reactor using a $SF_6$ /$O_2$ gas mixture using $SiO_2$ as a mask with a selectivity of 6.5. ~~Such process is known in the art and is disclosed, for example, in an article by F. Lanois, entitled "Angle Etch Control for Silicon Power Devices", which appeared in Applied Physics Letters, Vol 69, No. 2, pages 236-238, July 1996.~~ Alternatively, the SiC film can be etched by RIE using the mixture $SF_6$ and $O_2$ and $F_2/Ar/O_2$. ~~An example of such a process is disclosed in an article by N. J. Dartnell, et al., entitled "Reactive Ion Etching of Silicon Carbide" in Vacuum, Vol. 46, No. 4, pages 349-355, 1955.~~ The etch rate of the SiC film can be significantly increased by using magnetron enhanced RIE. Self-aligned source **205** and drain **210** regions can then be formed using conventional techniques for forming a FET **200** having a floating (electrically isolated) gate **215**, or in an alternate embodiment, an electrically interconnected (driven) gate.

**The paragraph beginning at page 26, line 10 is amended as follows:**

In one embodiment floating gate **215** is formed of a monocrystalline, polycrystalline, microcrystalline, or nanocrystalline, SiOC thin film that is CVD deposited, such as by a Two Consecutive Decomposition and Deposition Chamber (TCDDC) system. ~~One such example of depositing microcrystalline SiOC, in the unrelated technological field of solar cell applications, is disclosed in an article by R. Martins et al., entitled "Transport Properties of Doped Silicon~~

~~Oxycarbide Microcrystalline Films Produced By Spatial Separation Techniques," Solar Energy Materials and Solar Cells, Vol. 41-42, pp. 493-517, June 1996. See also an article by R. Martins et al., entitled "Wide band-gap microcrystalline silicon thin films," Diffusion and Defect Data Part B (Solid State Phenomena), Vol. 44-46, Pt. 2, pp. 299-346, 1995.~~

**The paragraph beginning at page 27, line 11 is amended as follows:**

In one embodiment, a composition $v$ of a polycrystalline $Ga_{1-v}Al_vN$ floating gate **215** is selected approximately between $0 < v < 1$ to obtain a desired barrier energy, as described below. The GaAlN floating gate **215** provides a lower electron affinity than polysilicon. The GaAlN floating gate **215** electron affinity can be approximately between 0.6 eV $< \chi_{215} <$ 2.7 eV as the GaAlN composition variable $v$ is decreased from 1 to 0. ~~See V. M. Bermudez et al. "The Growth and Properties of Al and AlN films on GaN" J. Appl. Physics, Vol. 79, No. 1, pp. 110-119 (1996).~~ As a result, the GaAlN floating gate **215** provides a smaller resulting barrier energy $\Phi_{GI}$ than a polysilicon gate material having an electron affinity $\chi_{215} \approx$ 4.2 eV. For example, using a $SiO_2$ gate insulator **225**, a barrier energy approximately between -0.3 eV $< \Phi_{GI} <$ 1.8 eV is obtained using an GaAlN floating gate **215** as the GaAlN composition $v$ varies between $v \approx 1$ (i.e., approximately AlN) and $v \approx 0$ (i.e., approximately GaN). By contrast, a conventional polysilicon floating gate material provides a barrier energy $\Phi_{GI} \approx$ 3.3 eV at an interface with an $SiO_2$ gate insulator **225**.

**The paragraph beginning at page 28, line 5 is amended as follows:**

In one embodiment floating gate **215** is formed of a polycrystalline, microcrystalline, or nanocrystalline, GaN thin film that is CVD deposited on a thin (e.g., 500 Å thick) AlN buffer layer, such as by metal organic chemical vapor deposition (MOCVD), which advantageously yields improved crystal quality and reduced microscopic fluctuation of crystallite orientation. ~~See e.g., V. M. Bermudez et al. "The Growth and Properties of Al and AlN films on GaN" J. Appl. Physics, Vol. 79, No. 1, pp. 110-119 (1996). See also I. Akasaki et al. "Effects of AlN Buffer Layer on Crystallographic Structure and On Electrical and Optical Properties of GaN and $Ga_{1-x}Al_xN$ Films Grown on Sapphire Substrate by MOVPE," J. Of Crystal Growth, Vol. 98, pp.~~

~~209-19, North Holland, Amsterdam (1989).~~

**The paragraph beginning at page 29, line 12 is amended as follows:**

~~The present invention provides a DEAPROM cell. The~~ Each memory cell described herein has a floating electrode, such as a floating gate electrode in a floating gate field-effect transistor. According to one aspect of the invention, a barrier energy between the floating electrode and the insulator is lower than the barrier energy between polysilicon and $SiO_2$, which is approximately 3.3 eV. ~~The~~ Each memory cell also provides large transconductance gain, which provides a more easily detected signal and reduces the required data storage capacitance value. According to another aspect of the invention, the shorter retention time of data charges on the floating electrode, resulting from the smaller barrier energy, is accommodated by refreshing the data charges on the floating electrode. By decreasing the data charge retention time and periodically refreshing the data, the write and erase operations can be several orders of magnitude faster. In this respect, ~~the~~ each memory operates similar to a memory cell in DRAM, but avoids the process complexity, additional space needed, and other limitations of forming stacked or trench DRAM capacitors.